DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to channel embedding [which suppressed the short channel effect] type a CMOS (Complementary Metal Oxide Semiconductor) type semiconductor device and its manufacture method about an MOS type semiconductor device.
[0002]
[Description of the Prior Art] In order to reduce the power consumption of VLSI, CMOS which is a low power type device is used. CMOS is the device which n channel MOS FET and p channel MOS FET are made [device] in one substrate, and was made to carry out complementary operation of the MOSFET of each above Although the aforementioned CMOS device is low power very much, it is one of the big technical problems on a process device design how since it is complicated compared with other MOS devices, the manufacture process completes these devices on the same substrate.
[0003] n type polycrystal silicon is used for both usual CMOS as a gate electrode of an n channel and a p channel. This is because a manufacturing cost can be reduced by using the same gate electrode. In this case, the threshold by the side of a p channel will become high too much. For this reason, a p-channel side is preparing an embedding layer, and makes almost equal the absolute value of the threshold by the side of an n channel and a p channel. Consequently, an n channel serves as a surface type MOSFET, and a p channel serves as embedding type MOSFET.
[0004] However, the problem of a short channel effect that the absolute value of threshold voltage falls is actualizing with detailed-izing of the channel length of MOSFET used for VLSI. By embedding type MOSFET, compared with the surface type MOSFET, the short channel effect became remarkable and it was thought that the cut off characteristic of sub threshold level current deteriorated (155 reference : Koyanagi, the "submicron device I" Maruzen, p. 1987).
[0005] Then, recently, the CMOS device which made the n channel and the p channel the surface type is used. Drawing 4 shows the cross section of the conventional CMOS device. p type well field 3 and the p-type-silicon source drain field 23 are formed in the silicon substrate 1, and, as for the aforementioned CMOS device, n type silicon source drain field 21 is further formed in the aforementioned p type well field 3. Here, both aforementioned n type silicon source drain field 21 and p-type-silicon source drain field 23 are separated by the isolation oxide film 5, and aforementioned both source and drain field are formed with the interval.
[0006] On the aforementioned silicon substrate 1, n type gate electrode 27 is formed through the gate oxide film 25 of n type silicon source drain field 21 which extends to a front face, and this in part. Similarly, on p type well field 3, p type gate electrode 29 is formed through the gate oxide film 25 and this of n type silicon source drain field 23 which extend to a front face in part.
[0007]
[Problem(s) to be Solved by the Invention] However, the trouble of the following [CMOS / which made both an n channel and p channel MOS FET the surface type MOSFET] is mentioned.
[0008] Above CMOS has the problem that change of the property by the variation in manufacture processes, such as gate oxide-film thick formation, becomes remarkable. Aggravation of productivity will be brought about if change of this property also becomes remarkable. Especially, since change of threshold voltage is so remarkable that gate length is short, it is a serious problem about the correspondence to detailed-izing of future VLSI.
[0009] Moreover, although Above CMOS has little influence of a short channel effect at a present stage in the present when detailed-ization of VLSI progresses at an increasing tempo, it has a fear of becoming a problem in the future. Therefore, development of a device with still less influence of a short channel effect is desired.
[0010] this invention is made in view of the aforementioned situation, and the place made into the purpose suppresses a short channel effect, and aims at offering the high semiconductor device and its manufacture method of the resistance over the variation in a manufacture process.
[0011]
[Means for Solving the Problem] In order to attain the above-mentioned purpose the 1st feature of the 1st invention In the semiconductor device which has n channel MOS FET and p channel MOS FET which were formed on the semiconductor substrate The gate electrode of aforementioned n channel MOS FET which consists of a p type polycrystal silicon film, It is having the gate electrode of aforementioned p channel MOS FET which consists of an n type polycrystal silicon film, and the embedding layer which was formed in the channel field of aforementioned n channel MOS FET and aforementioned p channel MOS FET and which is the same conductivity type as each source drain field.

[0012] Moreover, the 2nd feature of the 1st invention is making the aforementioned embedding layer into the thickness more than the junction depth of a source drain.
[0013] Furthermore, the feature of the 2nd invention is set to the method of manufacturing the semiconductor device which has n channel MOS FET and p channel MOS FET which were formed on the semiconductor substrate. The process which forms n type polycrystal silicon film on the formation field of n channel MOS FET, The process which forms p type polycrystal silicon film on the formation field of p channel MOS FET, The process which diffuses an impurity from described [above] n type and p type polycrystal silicon film, forms n type embedding layer in the channel field of n channel MOS FET, and forms p type embedding layer in the channel field of p channel MOS FET, The process which carries out patterning of described [above] n type and the p type polycrystal silicon film, and forms n type and p type source drain field, The process which oxidizes the aforementioned embedding layer, and described [above] n type and p type source drain field, and forms a gate oxide film, It is including the process which forms p type polycrystal silicon film used as the gate electrode of n channel MOS FET, and n type polycrystal silicon film used as the gate electrode of p channel MOS FET on this gate oxide film.
[0014] Here, as for the gate electrode of aforementioned p channel MOS FET, it is desirable to use the polycrystal silicon which poured in the element of an III group system, and it is good to use boron in that a high-concentration diffusion layer can be formed also in the element of the aforementioned III group system. Moreover, as for the gate electrode of aforementioned n channel MOS FET, it is desirable to use the polycrystal silicon which poured in the element of V group system, and it is good to use phosphorus in that a difference with the value of the diffusion coefficient of the aforementioned boron is small also in the element of the aforementioned V group system.
[0015] moreover, the point that a p type thing is desirable in the embedding layer by the side of the gate electrode of aforementioned n channel MOS FET, it is desirable to diffuse the element of an III group system and to make it form further, and a high-concentration diffusion layer can be formed especially -- **** for boron -- things are desirable It is desirable to use phosphorus on the other hand in that an n type thing is desirable in the embedding layer by the side of the gate electrode of aforementioned p channel MOS FET, it is desirable to diffuse the element of V group system and to use it further, and a difference with the value of the diffusion coefficient of the aforementioned boron is small especially.
[0016] moreover, in the process which forms n type polycrystal silicon film on the formation field of n channel MOS FET, forming with patterning technology is desirable, it is desirable to use the element of V group system further, and n type polycrystal silicon film is formed by carrying out the ion implantation of the phosphorus especially -- a thing is desirable
[0017] Moreover, in the process which forms p type polycrystal silicon film on the formation field of p channel MOS FET, it is desirable to use the element of an III group system, and it is desirable by carrying out the ion implantation of the boron especially to form p type polycrystal silicon film.
[0018] Moreover, the process which diffuses an impurity from the aforementioned polycrystal silicon film has the desirable process which diffuses an impurity by annealing.
[0019]
[Function] Although it is desirable to receive control of only the gate as for the current on which switching elements, such as MOSFET, flow a channel, it will be influenced [the influence of a drain, and] of a substrate in practice. Therefore, the case where current flowed in a place with these influences being the minimum near the gate, i.e., the front face of a channel, was considered that there is least influence of a short channel effect. Therefore, it embedded from the former and it was thought compared with the surface type MOSFET that Mold MOSFET had a remarkable short channel effect.
[0020] However, when current flows the specific depth with an embedding layer, the bird clapper is reported for the influence of a short channel effect to the minimum (reference : the patent application number PH 05155413). That is, by preparing an embedding layer, since a depletion layer spreads, influence of a substrate can be made small. Therefore, the influence of a substrate is small in an embedding layer, and influence of a short channel effect can be made fewer than a surface type MOSFET by forming by the most suitable thickness that can carry out control by the gate. In addition, by making it thicker than it to the same extent as the junction depth of a source drain, embedding layer thickness can reduce the charge share (charge share) by the source drain most, and can suppress a short channel effect.
[0021] Moreover, gate electric field fall compared with a surface type MOSFET, the gate oxide-film thick dependency of threshold voltage becomes weaker, and embedding type MOSFET can strengthen resistance over the variation in the aforementioned oxidization thickness. For this reason, change of the threshold voltage by the variation in channel length also becomes small.
[0022]
[Example] Hereafter, the example of the semiconductor device concerning this invention is explained based on a drawing. Drawing 1 shows the cross section of the aforementioned semiconductor device. p type well field 3 which the aforementioned semiconductor device is the interior of a silicon substrate 1 and this silicon substrate 1, and was formed in the front face, The isolation oxide film 5 formed so that the part might be embedded to the aforementioned silicon substrate 1 and the aforementioned p type well field 3, p type embedding layer 9 which was formed in the surface section of the aforementioned p type well field 3 and which embedded and was formed in a layer 7 and the surface section of the aforementioned silicon substrate 1, n type polycrystal silicon source drain field 11 which is on the front face of the aforementioned n type embedding layer 7, and was formed with the fixed interval, The p-type-silicon source drain field 13 which is on the front face of the aforementioned embedding layer 9, and was formed with the fixed interval, The gate oxide film 15 in which it is on the front face of the aforementioned n type embedding layer 7, and the part extended to the aforementioned n type polycrystal silicon source drain field

11, It consists of p type gate electrode 17 formed through this, a gate oxide film 15 in which it is on the front face of p type embedding layer 9 similarly, and the part extended to the aforementioned p type polycrystal silicon source drain field 13, and an n type gate electrode 19 formed through this.

[0023] Next, the manufacture method of the semiconductor device concerning this invention is explained based on a drawing. Drawing 2 and drawing 3 are the cross sections of a CMOS device showing the manufacturing process concerning the example of this invention.

[0024] first, as shown in drawing 2 (a), after forming p type well field 3 in the n-type-semiconductor substrate 1 with well-known technology and forming an oxide film 5 in an isolation field by the LOCOS method which is common knowledge, the polycrystal silicon film 31 which has not added the impurity by 0.8 micrometers (0.3 micrometers to 1.0 micrometers are sufficient) in thickness is deposited on the whole surface Next, on the aforementioned polycrystal silicon film 31 on the aforementioned p type well field 3, a resist 33 is saved, the ion implantation of the boron is carried out by making this into a mask by for example, acceleration voltage 30KeV (50KeV(s) from 10KeV are sufficient), and pouring dose 5x1015cm-2 (1015cm-2 to 1016cm-2 is sufficient), and p type polycrystal silicon field 35 is formed.

[0025] Next, as shown in drawing 2 (b), on the aforementioned polycrystal silicon films 31 other than the aforementioned p type well field 3, a resist 39 is saved, the ion implantation of the phosphorus is carried out by making this into a mask by for example, acceleration voltage 30KeV (50KeV(s) from 10KeV are sufficient), and pouring dose 5x1015cm-2 (1015cm-2 to 1016cm-2 is sufficient), and n type polycrystal silicon field 37 is formed. Next, 800 degrees C (600 degrees C to 1000 degrees C are sufficient) annealing is performed in nitrogen atmosphere for 30 minutes (****** for 120 minutes after for 10 seconds). Phosphorus is diffused from n type polycrystal silicon field 37 to the aforementioned p well field 3. Boron is diffused from p type polycrystal silicon field 35 to the aforementioned n type substrate 1, and 30nm (10nm to 50nm is sufficient) formation of the p type embedding layer 9 as shown in drawing 2 (c) is carried out, for example at the same time it forms n type embedding layer 7 as shown in drawing 2 (c).

[0026] next, as shown in drawing 2 (c), n type polycrystal silicon field 11 is formed in the field which serves as a source drain of n channel MOS FET with well-known patterning technology, and p type polycrystal silicon field 13 is formed in the field used as the source drain which is p channel MOS FET

[0027] As shown in drawing 3 (d), the aforementioned n type embedding layer 7, the aforementioned p type embedding layer 9, the aforementioned n type polycrystal silicon source drain field 11, and the aforementioned p type polycrystal silicon source drain field 13 next, by oxidizing For example, after forming the 10nm (5nm to 20nm is sufficient) thermal oxidation film 15, For example, the polycrystal silicon film which has not added the impurity by 0.8 micrometers (0.3 micrometers to 1.0 micrometers are sufficient) in thickness is deposited on the whole surface. The ion implantation of the boron is carried out by for example, acceleration voltage 30KeV (50KeV(s) from 10KeV are sufficient), and pouring dose 5x1015cm-2 (1015cm-2 to 1016cm-2 is sufficient), and p type gate polycrystal silicon field 41 is formed. Next, the CVD film 45 is saved on this p type gates polycrystal silicon film 41 on the aforementioned p type well field 3, phosphorus is diffused by making this into a mask, and n type gate polycrystal silicon film 43 is formed. This CVD film 45 after formation is removed.

[0028] Next, as shown in drawing 3 (e), p type gate electrode 17 and n type gate electrode 19 are formed with well-known patterning technology. After depositing a CVD oxide film on the whole surface according to the usual process and forming a protective coat hereafter, a contact hole is punctured, an aluminum electrode is formed and a CMOS device is formed.

[0029] Thus, by embedding an n channel and a p channel and consisting of molds MOSFET, gate electric field fell compared with the surface type MOSFET, and the resistance of the CMOS device manufactured over the variation in the gate oxidization film pressure of threshold voltage improved. Moreover, by carrying out thickness of an embedding layer more than the junction depth of a source drain, the charge share (charge share) by the source drain was able to decrease, and the short channel effect was also able to be suppressed.

[0030] this invention is not limited to the above-mentioned example at all, and may be suitably changed in the range which does not deviate from the summary of invention.

[0031]

[Effect of the Invention] As explained above, according to this invention, by embedding an n channel and a p channel and consisting of molds MOSFET, the resistance over the variation in a manufacture process is strong, and can realize the highly efficient CMOS device which can suppress a short channel effect.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the structure section view of the semiconductor device concerning this invention.
[Drawing 2] It is the process cross section (first portion) showing the manufacturing process of the example concerning this invention.
[Drawing 3] It is the process cross section (second half section) showing the manufacturing process of the example concerning this invention.
[Drawing 4] It is the structure section view of the conventional semiconductor device.
[Description of Notations]
1 Silicon Substrate
3 P Type Well Field
5 Isolation Oxide Film
7 N Type Embedding Layer
9 P Type Embedding Layer
11 N Type Polycrystal Silicon Source Drain Field
13 P Type Polycrystal Silicon Source Drain Field
15 25 Gate oxide film
17 29 p type gate electrode
19 27 n type gate electrode
21 N Type Silicon Source Drain Field
23 P-Type-Silicon Source Drain Field
31 Polycrystal Silicon Film
33 39 Resist film
35 41 p type polycrystal silicon film
37 43 n type polycrystal silicon film
45 CVD Film

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the MOS type field-effect transistor (MOSFET) used for the analog circuit section or the circuit section which loaded together the analog circuit and the digital circuit simultaneously.
[0002]
[Description of the Prior Art] Complementary MOS FET (it omits Following CMOS) used for an integrated circuit device is constituted by p channel MOS FET and n channel MOS FET. It is the material conventionally used for a gate electrode n+ Whether it considers as contest polysilicon, and p+ CMOS considered only two kinds of composition as follows by whether it considers as contest polysilicon. Namely, (1) It is n+ to a gate electrode. If contest polysilicon is used, n channel MOS FET will serve as a surface channel type, and p channel MOS FET will serve as an embedding channel type.
(2) It is n+ to a gate electrode. Contest polysilicon and p+ When contest polysilicon is used, respectively, n channel MOS FET is n+. Becoming a surface channel type by the poly silicon gate, p channel MOS FET is p+. It becomes a surface channel type by the poly silicon gate.
[0003] It is (2) here. It is n+ like. Contest polysilicon and p+ If contest polysilicon is used, a CMOS manufacturing process will become complicated and will raise a manufacturing cost. However, this CMOS can use p channel MOS FET as a surface channel type, and is advantageous to a short channel effect. Generally, if MOSFET is made detailed below in a submicron region, the phenomenon of the fall of threshold voltage (it is described as threshold voltage and Following Vth), increase of the drain voltage dependency of Vth, and increase of the leakage current of a sub threshold level region etc. will appear, and the bad influence to these detailed-izing is called short channel effect. To this short channel effect showing up, the surface channel type is stronger than an embedding channel type by making it detailed. For the direction of a surface channel type, drain current is [it] SiO2/Si. It is the shell which flows near the interface and cannot be easily influenced of drain voltage.
[0004] It can respond also to detailed-ization to a submicron region by devising also by embedding channel type p channel MOS FET, in fact, as shown in the view 7 (drawing 9 in this explanation) proposed, for example by JP,4-82064,B. in addition, drawing 9 -- setting -- 16 -- for a gate oxide film and 19, as for the source / drain field, p type channel field of this conductivity type, and 21, a side-attachment-wall oxide film and 20 are [p type source / drain field, and 17 / a gate electrode and 18 / n type high concentration impurity layer of a channel field and an opposite conductivity type and 22] n type wells By forming the high concentration impurity layer 21, embedding p-channel type MOSFET of this drawing 9 suppresses the potential elongation by drain voltage, and a certain grade can suppress a short channel effect. However, it essentially embeds and a channel type is weak to a short channel effect. Then, it is in the inclination to also use p channel MOS FET as an advantageous surface channel type to detailed-izing, in the circuit which can ask for high speed like a digital circuit, high accumulation, and low-power-ization.
[0005] By the way, about MOSFET used for an analog circuit, stabilization of a process and highly-precise-izing are more important than detailed-izing. That is because dispersion (pair nature of MOSFET etc.) by the manufacturing process of MOSFET links with ** and circuit performance degradation directly in an analog circuit. For this reason, generally the gate length of MOSFET used for an analog circuit is maintaining the performance as several micrometers or more. This is the point that are a value large enough compared with the gate length (1 micrometer or less) of MOSFET used for a digital circuit, and an improvement is desired.
[0006] Moreover, as a performance required of CMOS for analog circuits, there is an internal noise of MOSFET other than the pair nature of MOSFET. Especially, compared with a bipolar transistor, the internal noise of MOSFET is large, and it has a problem practically. (1) described previously Although improvement which observed these at detailed-ization was carried out when both n channel MOS FET [like the case where a surface channel type and p channel MOS FET embed, and are a channel type, and (2)] whose n channel MOS FET [like] is, and p channel MOS FET were surface channel types, improvement in the viewpoint of reduction of an internal noise was not made. It is a thing for the purpose (detailed-ization is attained) which suppresses a short channel effect also about aforementioned JP,4-82064,B, and reduction of an internal noise is not considered. For this reason, the method of enlarging gate area as a method of reducing an internal noise by MOSFET was taken conventionally. generally, it is reported that the internal noise of MOSFET is in inverse proportion to gate area -- having -- **** (for example, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.ED-29, NO.6, and JUNE 1982) -- in addition -- being alike -- gate area was enlarged, since there was no effective method of reducing an internal noise in order to reduce an internal noise, and in order to raise the pair nature of MOSFET Therefore, there was a problem that raising a degree of integration

especially in an analog circuit was checked on the noise problem. Moreover, in the analog circuit from which an internal noise poses a problem, the bipolar transistor using the crystalline good field understood [of the noise] are few has been used.
[0007] By the way, when both the analog circuit section and the digital circuit section were constituted from the circuit (an analog / digital mixed-loading circuit) consolidated with the analog circuit and the digital circuit by CMOS, the composition of CMOS of the digital circuit section was conventionally used to the analog circuit section as it was. Namely, (1) described previously When a surface channel type and p channel MOS FET embed and n channel MOS FET [like] is a channel type, the digital circuit section and the analog circuit section are (1). The composition of CMOS was used. Moreover, (2) described previously It is (2) although p channel MOS FET was used as the surface channel type for the performance (the high speed by detailed-izing of an element, high accumulation, low-power-izing) primarily required of the digital circuit section when both n channel MOS FET [like] and p channel MOS FET were surface channel types. The composition of CMOS has been used not only for the digital circuit section but for the analog circuit section. For this reason, special means to reduce the internal noise of the analog circuit section were not taken, but in order to reduce an internal noise, they enlarged gate area of the analog circuit section. As for the analog circuit section, the circuit where CMOS is used is taken in the case where an internal noise still poses a problem, as for a bipolar transistor and the digital circuit section.
[0008]
[Problem(s) to be Solved by the Invention] However, although it said that gate area is enlarged in order to reduce an internal noise when CMOS was used in an analog circuit, this increased the chip area of an analog circuit and had the trouble of raising product cost. Furthermore, when gate area was enlarged, gate oxide-film capacity, the junction capacitance of the source and a drain, etc. increased, and while the phenomenon of reducing a working speed arose, there was also a trouble of increasing power consumption. Moreover, when a bipolar transistor was used in an analog circuit, in order that a bipolar transistor might pass a base current and might operate an element, it had the trouble that power consumption was large and could not enlarge an input impedance further in essence compared with CMOS. And generally, there was a process which grows silicon epitaxially and there was also a trouble that a manufacturing cost was higher than a CMOS manufacturing process on a silicon substrate at the manufacturing process of a bipolar transistor for this process.
[0009] Moreover, in an analog / digital mixed-loading circuit, when both the analog circuit section and the digital circuit section are manufactured with CMOS, in order to reduce the noise of the analog circuit section, gate area of MOSFET of the analog circuit section needed to be enlarged, after all, chip area was increased and there was a trouble of raising a manufacturing cost. Furthermore, when gate area was enlarged, gate oxide-film capacity, the junction capacitance of the source and a drain, etc. increased, and there was also a trouble of the fall of a working speed and increase of power consumption. Moreover, in an analog / digital mixed-loading circuit, it was a bipolar transistor about the analog circuit section, when the digital circuit section was manufactured with CMOS, two kinds of manufacturing processes, the manufacturing process of a bipolar transistor and the manufacturing process of CMOS, were needed to the same chip, for this reason, the manufacturing process became very complicated, and there was a problem of raising a manufacturing cost sharply. Furthermore, the problem of power consumption or an input impedance also exists. Moreover, (2) previously described in the analog / digital mixed-loading circuit When both n channel MOS FET and p channel MOS FET are used as a surface channel type like, Although the performance (the high speed by detailed-izing of an element, high accumulation, low-power-izing) required of the digital circuit section can be satisfied There was a trouble that a different performance which cannot be satisfied about the performance (reduction of an internal noise and reduction of gate area) required of the analog circuit section, that is, is required of the analog circuit section and the digital circuit section could not be satisfied simultaneously.
[0010] Therefore, the purpose of this invention is offering the composition which reduces the internal noise of CMOS used for the analog circuit section in an analog circuit, and an analog / digital mixed-loading circuit, and offering CMOS for analog circuits which can attain simultaneously reduction of the internal noise of CMOS, and reduction of gate area. Moreover, the purpose of this invention is offering CMOS for analog circuits which enables it to be managed even if it does not use a bipolar transistor for the analog circuit section on the problem of an internal noise in an analog circuit, and an analog / digital mixed-loading circuit. Furthermore, the purpose of this invention is offering CMOS an analog / for digital mixed-loading circuits with which are simultaneously satisfied of the performance (reduction of an internal noise, and reduction of gate area) required of the analog circuit section in an analog / digital mixed-loading circuit, and the performance (the high speed by detailed-izing of an element, high accumulation, low-power-izing) required of the digital circuit section.
[0011]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the transistor of the analog circuit section of this invention consists of CMOS, and the composition of this invention is n+ in a gate electrode. Contest polysilicon and p+ Contest polysilicon is used, respectively and n channel MOS FET is p+. It embeds by using the poly silicon gate, and is made the n channel type, and p channel MOS FET is embedded by using n+ poly silicon gate, and is used as the p-channel type. Moreover, the transistor of an analog / digital mixed-loading circuit consists of CMOS, and another composition is n+ in a gate electrode. Contest polysilicon or p+ Contest polysilicon is used and n channel MOS FET of the analog circuit section is p+. It embeds by using the poly silicon gate, and is made the n channel type, and p channel MOS FET is n+. It embeds by using the poly silicon gate, and is made the channel type. And n channel MOS FET of the digital circuit section is n+. By using the poly silicon gate, it is made the surface channel type and p channel MOS FET is p+. It is the feature by using the poly silicon gate to have made it the surface channel type.
[0012]

[Function] It explains that the operation of this invention is made based on the experiment fact shown below. Drawing 8 is as a result of [of the internal noise of MOSFET of a surface channel type and each embedding channel mold] measurement. The internal noise is shown in the vertical axis as input conversion noise-voltage density in 10Hz. Moreover, a horizontal axis is a gate voltage Vg. It is shown and what the threshold voltage Vth is deducted for (absolute value of Vg-Vth) has rectified gap of Vth of an element. Since the element in an analog circuit is used by the saturation region as measurement conditions, the internal noise has been measured by the saturation region to each gate voltage. A solid line is as a result of [of surface channel type MOSFET] measurement, and a dashed line is as a result of [of embedding channel type MOSFET] measurement. Gate length, gate width, and gate oxidization thickness are both the same setup. It is clear that a result's embedding channel type of an internal noise is smaller about 70% at the maximum with the channel type embed to every gate voltage and smaller [an internal noise] and.
[0013] This is explained as follows qualitatively. In surface channel type MOSFET, drain current flows near the SiO2/Si interface. It embeds to it, and drain current spreads and flows from near the SiO2/Si interface in channel type MOSFET. Moreover, there are many lattice defects near the SiO2/Si interface, a lattice defect captures at random the carrier of current which is flowing, and emits a channel field, the density fluctuation of current occurs by this, and it is thought that the internal noise has occurred. From these things, since embedding channel type MOSFET spreads from near the SiO2/Si interface and current is flowing, it compares with a surface channel type, it is thought that it is hard to be influenced of [near the SiO2/Si interface], and it is predicted that an internal noise is small. It was shown by the survey data of drawing 8 that this prediction is almost right.
[0014]
[Effect of the Invention] It is based on this experiment fact and is a book. Since according to the claim 1 of this invention p type and n type were embedded and it considered as channel type composition, current flows the field where each channel is deep, and it becomes the complementary-type insulated-gate field-effect transistor which an internal noise cannot generate easily. Moreover, according to the claim 2, the circuit where the internal noise raised the degree of integration with a small gate area few compared with the analog circuit of the conventional CMOS composition is realized. Moreover, since according to the claim 3 it embeds in an analog / digital mixed-loading circuit] at an analog circuit and a channel type is used, the internal noise in an analog circuit is reduced. The performance required of performances, such as the rapidity required of the digital circuit section by embedding in / an analog / a digital mixed-loading circuit / as there is the reduction effect of the interior noise which depends what forms an embedding channel type and surface channel type simultaneously according to the claim 4 furthermore on an embedding channel type and it is shown in a claim 5] in the analog circuit section, and using a surface channel type for the channel type and digital circuit section, and the analog circuit section can satisfy simultaneously.
[0015] That is, (1) stated with the conventional technology by embedding n channel MOS FET and p channel MOS FET, and making it a channel type in the analog circuit section of an analog circuit, and an analog / digital mixed-loading circuit When like, the internal noise of n channel MOS FET is sharply reduced by n channel MOS FET's embedding and being made a channel type. Moreover, (2) stated with the conventional technology When like, n channel MOS FET and p channel MOS FET reduce an internal noise sharply by using both n channel MOS FET and p channel MOS FET as an embedding channel type.
[0016] In an analog / digital mixed-loading circuit And n channel MOS FET of the analog circuit section, If p channel MOS FET is embedded, it is made a channel type and n channel MOS FET of the digital circuit section and p channel MOS FET are used as a surface channel type The performance (reduction of an internal noise and reduction of gate area) required of the analog circuit section can be embedded, and it can be satisfied with a channel type, and can be satisfied [with a surface channel type] of the performance (the high speed by detailed-izing of an element, high accumulation, low-power-izing) required of the digital circuit section. It is alike, and it compares, an internal noise can be reduced, and gate area can be simultaneously made small. While this avoids the cost elevation by increase of chip area, improvement in a working speed and low-power-ization can be attained.
[0017] Moreover, when the bipolar transistor is being conventionally used for the analog circuit section, reduction of a low power, a high input impedance, and a manufacturing cost can be realized to composition conventionally which may be able to manufacture with CMOS by applying this invention, and uses a bipolar transistor in this case. When it can manufacture with CMOS by using this invention compared with the case where the analog circuit section was manufactured by the bipolar transistor, and the digital circuit section is manufactured with CMOS especially in an analog / digital mixed-loading circuit, a manufacturing cost can be reduced sharply. Therefore, the analog / digital mixed-loading circuit of the CMOS composition with which it is simultaneously satisfied of a different performance required of the analog circuit section and the digital circuit section with the composition of this invention are realizable.
[0018]
[Example] Hereafter, this invention is explained based on a concrete example. Drawing 1 is the typical composition cross section of CMOS used for the analog circuit of this invention. In drawing 1 , the n type Si well 2 and the p type Si well 3 are formed in the Si substrate 1, the p+ type Si source / drain 4 is formed on the n type Si well 2, and it is n+. The type Si source / drain 5 is formed on the p type Si well 3. Moreover, p - The type channel field 6, n - The type channel field 7 is formed between each source / drain section, and is separated by the Si oxide film 8 for separation between elements (LOCOS oxide film). In addition, like the structure looked at by usual CMOS, they are the gate Si oxide film 9, the side-attachment-wall oxide film 10, and n+. The type poly silicon-gate electrode 11 and p+ The type poly silicon-gate electrode 12, the metal silicide (silicide) 13, the layer insulation film 14, and the aluminum wiring 15 constitute MOSFET.
[0019] Drawing 2 - drawing 4 explain the manufacturing process of CMOS for analog circuits shown in drawing 1 . As first shown in drawing 2 , a process is usually followed on the Si substrate 1, and it is surface concentration 2.0x1016 (cm-3). The n type Si well 2 and surface concentration 2.0x1017 (cm-3) The p type Si well 3 is formed. After forming the Si oxide film

(LOCOS oxide film) 8 in isolation and forming the gate oxide film 9 of 160 **, On the n type Si well 2, it is boron (B) about the ion implantation for threshold voltage Vth control. 30KeV(s) and 1.0x1012 (cm-2) On conditions In the p type Si well 3, it is Lynn (P). 80KeV(s) and 3.5x1012 (cm-2) It carries out on conditions and is p. - The type Si channel field 6 and n - The type Si channel field 7 is formed, respectively.

[0020] next, volume of neutral (a non dope, high resistance) contest polysilicon is carried out by the chemical vapor deposition with well-known technology like drawing 3 -- making -- and -- contest polysilicon on the n type Si well 2 -- Lynn -- (P) contest polysilicon on the p type Si well 3 -- boron (B) an ion implantation -- carrying out -- alternative -- n+ The type poly silicon-gate electrode 11 and p+ The type poly silicon-gate electrode 12 is formed.

[0021] next, drawing 4 -- like -- usually -- a process -- following -- the chemical vapor deposition after forming an electric-field relief layer (not shown) -- SiO2 -- depositing -- etching removal -- carrying out -- the side-attachment-wall oxide film 10 -- forming -- self -- conformable -- the n type Si well 2 top -- p+ the type Si source / drain 4 -- the p type Si well 3 top -- n+ The type Si source / drain 5 is formed.

[0022] next, well-known technology -- self -- form silicide 13 conformably on the poly silicon gate 11, 12 tops, and the source/drain 4, and 5, and the layer insulation film 14 is made to deposit in a chemical vapor deposition, and after making the hole for contact which connects the source/drain, and aluminum wiring, the pattern vacuum evaporationo of the aluminum (aluminum) is carried out -- making -- the aluminum wiring 15 (drawing 1) -- forming -- drawing 1 -- it becomes Then, although not illustrated, according to a process, MOSFET is usually completed.

[0023] Thus, both n channel MOS FET and p channel MOS FET is also embedding channel types, and the manufactured analog circuit has a small internal noise compared with CMOS usually manufactured at a process.

[0024] (The second example) One example about CMOS used for the analog / digital mixed-loading circuit of this invention is explained using drawing 5 - drawing 7 . Drawing 5 is the composition cross section of typical CMOS with which the analog circuit section and the two digital circuit sections are put in order and formed in the same Si substrate 1. The Si substrate 1 separates into the analog circuit section and the digital circuit section, respectively, and the n type Si well 2 and the p type Si well 3 are formed in it. And p+ To the n type Si well 2, the type Si source / drain 4 is n+ again. The type Si source / drain 5 is formed in the p type Si well 3, and it is p between each source/drain. - The type channel field 6, n - The layer of the type channel field 7 is formed. In addition, since the channel fields 6 and 7 of the analog circuit section serve as an embedding layer, respectively since a well differs from a conduction type, and they form the channel fields 6 and 7 of the digital circuit section in a well same conduction type, an embedding channel does not become, but merely serves as a layer as carrier concentration regulation, and commits them as a surface channel.

[0025] and the Si oxide film 8 for separation between elements (LOCOS oxide film) -- each -- it forms so that wells 2 and 3 may be separated -- having -- each channel field top -- respectively -- the gate Si oxide film 9 -- preparing -- n+ type poly silicon-gate electrode 11 -- p- the type channel field 6 top -- moreover, p+ the type poly silicon-gate electrode 12 -- n- On the type channel field 7, pattern formation is carried out and the side-attachment-wall oxide film 10 is formed at both the sides of each gate. And after covering source / drain field top by the thin film of the metal silicide (silicide) 13, all the Si substrate 1 upper surfaces are protected by the layer insulation film 14, opening used as contact of the source / drain section is prepared, the aluminum wiring 15 is formed there, and the analog / digital mixed-loading circuit CMOS is formed.

[0026] Drawing 6 and drawing 7 explain the manufacturing process of the analog / CMOS for digital mixed-loading circuits shown in drawing 5 . As shown in drawing 6 , a process is usually followed on the Si substrate 1, and it is surface concentration 2.0x1016 (cm-3). The n type Si well 2 and surface concentration 2.0x1017 (cm-3) The p type Si well 3 is formed, respectively. After forming the Si oxide film 8 for isolation (LOCOS oxide film) and forming the gate oxide film 9 of 160 **, About the ion implantation for threshold voltage Vth control, it is boron (B) on the n type Si well 2 of the analog circuit section. 30KeV(s) and 1.0x1012 (cm-2) On conditions Moreover, on p type well 3 of the analog circuit section, it is Lynn (P). 80KeV(s) and 3.5x1012 (cm-2) On conditions Furthermore on the n type Si well 2 of the digital circuit section, it is Lynn (P). 80KeV(s) and 2.0x1012 (cm-2) On conditions And on p type well 3 of the digital circuit section, it is boron (B). 30KeV(s) and 2.0x1011 (cm-2) It carries out on conditions and they are the p- type Si channel field 6 and n. - The type Si channel field 7 is formed, respectively.

[0027] Next, neutral (a non dope, high resistance) contest polysilicon is made to deposit in a chemical vapor deposition with well-known technology like drawing 7 . In polysilicon contest 11a on the n type Si well 2 of the analog circuit section, it is Lynn (P). An ion implantation is carried out. polysilicon contest 12a on the p type Si well 3 of the analog circuit section -- boron (B) contest polysilicon on the n type Si well 2 of the digital circuit section -- 12d -- boron (B) and contest polysilicon on the p type Si well 3 of the digital circuit section -- 11d -- Lynn -- (P) An ion implantation is carried out. It is n+ alternatively. The type poly silicon-gate electrode 11 and p+ Pattern formation of the type poly silicon-gate electrode 12 is carried out. By manufacturing by the same manufacture method as the 1st example, an analog / CMOS for digital mixed-loading circuits as shown in drawing 5 can be obtained after this.

[0028] Thus, the analog circuit section embeds the analog / digital mixed-loading circuit which manufactured, an internal noise is small at a channel type, and the digital circuit section has structure which was suitable for detailed-ization with the surface channel type, and does not almost complicate a manufacturing process.

[0029] As explained above, CMOS for analog circuits by this invention embeds n channel MOS FET and p channel MOS FET, and is a channel type, and it is possible to realize CMOS which attains reduction of an internal noise and reduction of gate area simultaneously. Moreover, it is also possible for the analog circuit section to embed the analog / digital mixed-loading circuit by this invention, it to have become a channel type, and to realize the analog / digital mixed-loading circuit of CMOS with which are

simultaneously satisfied of a different performance required of the analog circuit section and the digital circuit section.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The 1st example of this invention is shown. Typical cross section of CMOSFET.
[Drawing 2] The typical cross section of the manufacturing process of the 1st example of this invention (the 1).
[Drawing 3] The typical cross section of the manufacturing process of the 1st example of this invention (the 2).
[Drawing 4] The typical cross section of the manufacturing process of the 1st example of this invention (the 3).
[Drawing 5] The 2nd example of this invention is shown. Typical cross section of CMOSFET.
[Drawing 6] The typical cross section of the manufacturing process of the 2nd example of this invention (the 1).
[Drawing 7] The typical cross section of the manufacturing process of the 2nd example of this invention (the 2).
[Drawing 8] Drawing in which explaining the principle of this invention and showing the measurement result of the internal noise of an embedding channel type and a surface channel type.
[Drawing 9] The cross section of the conventional embedding channel type MOSFET improved to detailed-izing.
[Description of Notations]
1 .. Si substrate
2..n type Si well
3..p type Si well
4 .. the p+Si source / drain
5 .. the n+Si source / drain
6 .. a p-Si channel field (the analog section is an embedding type and the digital section is a surface type)
7 .. an n-Si channel field (the analog section is an embedding type and the digital section is a surface type)
8 .. Si oxide film for separation between elements (LOCOS oxide film)
9 .. a gate Si oxide film
10 .. a side-attachment-wall oxide film
11 .. n+ Type poly silicon-gate electrode
12 .. p+ Type poly silicon-gate electrode
13 .. a metal silicide (silicide)
14 .. a layer insulation film
15 .. aluminum wiring
16..p type source / drain
17 .. a gate electrode
18 .. a gate oxide film
19 .. a side-attachment-wall oxide film
20 .. the source / drain field, and p type channel field of this conductivity type
21 .. n type high concentration impurity of a channel field and an opposite conductivity type
22..n type well

[Translation done.]